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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Applicant Kayvan Sadra, et al.

Docket Number: TI-35961

Serial No.: 10/694,237

Art Unit: 2813

Filed: 10/27/03

Examiner: Laura M. Schillinger

For: Application of Different Isolation Schemes for Logic and
Embedded Memory

CERTIFICATION OF FACSIMILE TRANSMISSION

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FACSIMILE COVER SHEET

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<input type="checkbox"/> CONTINUATION APP'N	<input checked="" type="checkbox"/> ELECTION
<input type="checkbox"/> DIVISIONAL APP'N	
NAME OF INVENTOR(S): Kayvan Sadra, et al.	
TITLE OF INVENTION: Application of Different Isolation Schemes for Logic and Embedded Memory	
TI FILE NO.: TI-35961	DEPOSIT ACCT. NO.: 20-0668
FAXED: 1-10-05 DUE: 1-30-05 ATTY/SECY: RAK/kjv	
RECEIPT DATE & SERIAL NO.: Serial No.: 10/694,237 Filing Date: 10/27/03	

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

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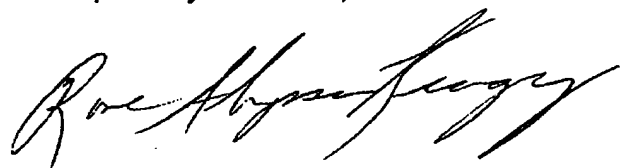
ELECTION

This election is offered in response to the Examiner's restriction requirement mailed December 30, 2004.

Applicants hereby provisionally elect to pursue the first invention with Claims 1-25, without traverse.

Respectfully submitted,

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